



## **FAST KNN CLASSIFICATION BASED ON SOFTCORE CPU AND RECONFIGURABLE HARDWARE**

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**ABSTRACT**—This paper presents a novel architecture for  $k$ -nearest neighbor ( $k$ NN) classification using field programmable gate array (FPGA). In the architecture, the first  $k$  closest vectors in the design set of a  $k$ NN classifier for each input vector are first identified by performing the partial distance search (PDS) in the wavelet domain. To implement the PDS in hardware, subspace search, bitplane reduction, multiple-coefficient accumulation and multiple-module computation techniques are employed for the effective reduction of the area complexity and computation latency. The proposed implementation has been embedded in a softcore CPU for physical performance measurement. Experimental results show that the implementation provides a cost-effective solution to the FPGA realization of  $k$ NN classification systems where both high throughput and low area cost are desired.

**Key Words:**  $k$ NN, partial distance search, FPGA, reconfigurable computing